ABSTRACT OF THE DISCLOSURE

A method for forming metal salicide regions and metal salicide exclusion regions in an integrated circuit (IC) that requires a minimum number of steps and is compatible with standard MOS processing techniques. An IC structure is first provided, with the IC structure including a plurality of MOS transistor structures with exposed silicon surfaces, such as source regions, drain regions and polysilicon gates. A metal layer (e.g., cobalt, titanium, tantalum, nickel or molybdenum) is then deposited over the IC structure in a controlled manner. A photoresist masking layer is then formed on those MOS transistor structures where metal salicide regions are to be formed. The metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed is then removed. The photoresist masking layer is then stripped from those MOS transistor structures where metal salicide regions are to be formed, and metal (in the remaining portions of the metal layer) that is in direct contact with silicon in the exposed silicon surfaces is then reacted to form metal salicide regions. By appropriately controlling parameters of the metal layer deposition step, the metal to be reacted to produce metal salicide, and the metal salicide resulting from the reaction, are caused to have desired properties or attributes. For example, where the metal salicide formation step is a step in forming a polysilicon interconnection, the metal deposition step can be performed in a manner that results in a predetermined sheet resistance or conductivity of the polysilicon interconnection.